



PPTC144WM-Q

50 V, 100 mA NPN resistor-equipped transistor;
 $R1 = 47 \text{ k}\Omega$, $R2 = 22 \text{ k}\Omega$

27 June 2025

Product data sheet

1. General description

NPN Resistor-Equipped Transistor (RET) in an leadless ultra small SOT883 (SC-101) Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit applications

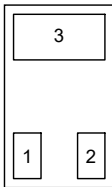
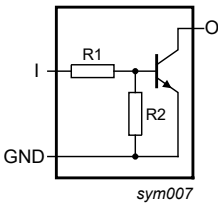
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current		-	-	100	mA
R1	bias resistor 1 (input)	$T_{amb} = 25 \text{ }^{\circ}\text{C}$	33	47	61	$\text{k}\Omega$
R2/R1	bias resistor ratio		0.37	0.47	0.57	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 Transparent top view DFN1006-3 (SOT883)	 sym007
2	GND	ground (emitter)		
3	O	output (collector)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PDTC144WM-Q	DFN1006-3	plastic, leadless ultra small package; 3 terminals; 0.35 mm pitch; 1 mm x 0.6 mm x 0.48 mm body	SOT883

7. Marking

Table 4. Marking codes

Type number	Marking code
PDTC144WM-Q	DD

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	10	V
V _I	input voltage			-10	40	V
I _O	output current			-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1] [2]	-	250	mW
T _J	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] Reflow soldering is the only recommended soldering method.
- [2] Device mounted on an FR4 PCB with 60 μm copper strip line, standard footprint.

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	500	K/W

- [1] Reflow soldering is the only recommended soldering method.
- [2] Device mounted on an FR4 PCB with 60 μm copper strip line, standard footprint.

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100\text{ }\mu\text{A}$; $I_E = 0\text{ A}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2\text{ mA}$; $I_B = 0\text{ A}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		50	-	-	V
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}$; $I_E = 0\text{ A}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	100	nA
		$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$; $T_j = 150\text{ }^{\circ}\text{C}$		-	-	5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}$; $I_C = 0\text{ A}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	110	μA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}$; $I_C = 5\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		60	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}$; $I_B = 0.5\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}$; $I_C = 100\text{ }\mu\text{A}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	1.7	1.2	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}$; $I_C = 2\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		4	2.7	-	V
R1	bias resistor 1 (input)	$T_{amb} = 25\text{ }^{\circ}\text{C}$		33	47	61	kΩ
R2/R1	bias resistor ratio			0.37	0.47	0.57	
C_c	collector capacitance	$V_{CB} = 10\text{ V}$; $I_E = 0\text{ A}$; $i_e = 0\text{ A}$; $f = 1\text{ MHz}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	2.5	pF

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

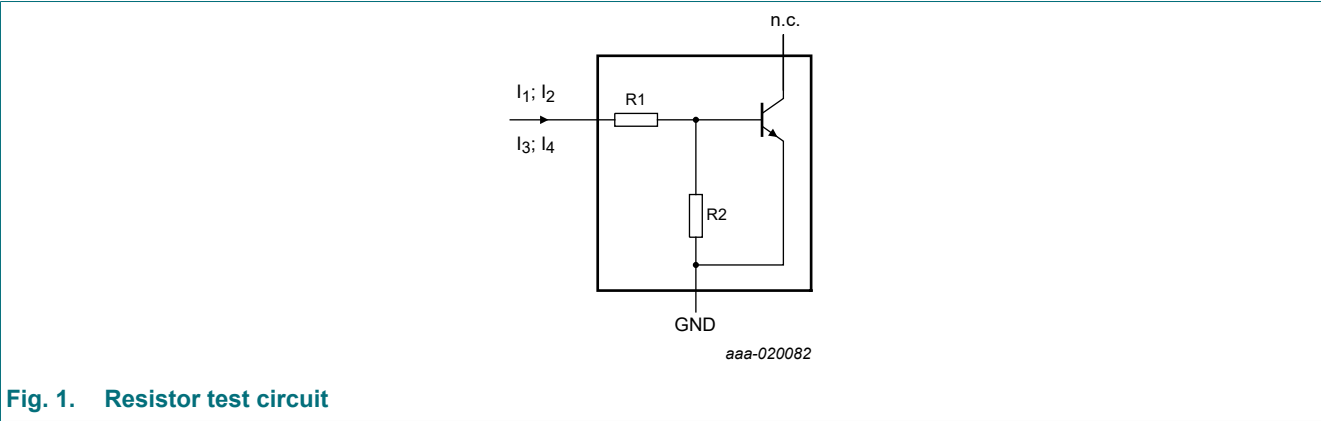


Fig. 1. Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I ₁	I ₂	I ₃	I ₄
PDTC144WM-Q	47	22	55 μA	105 μA	-55 μA	-105 μA

12. Package outline

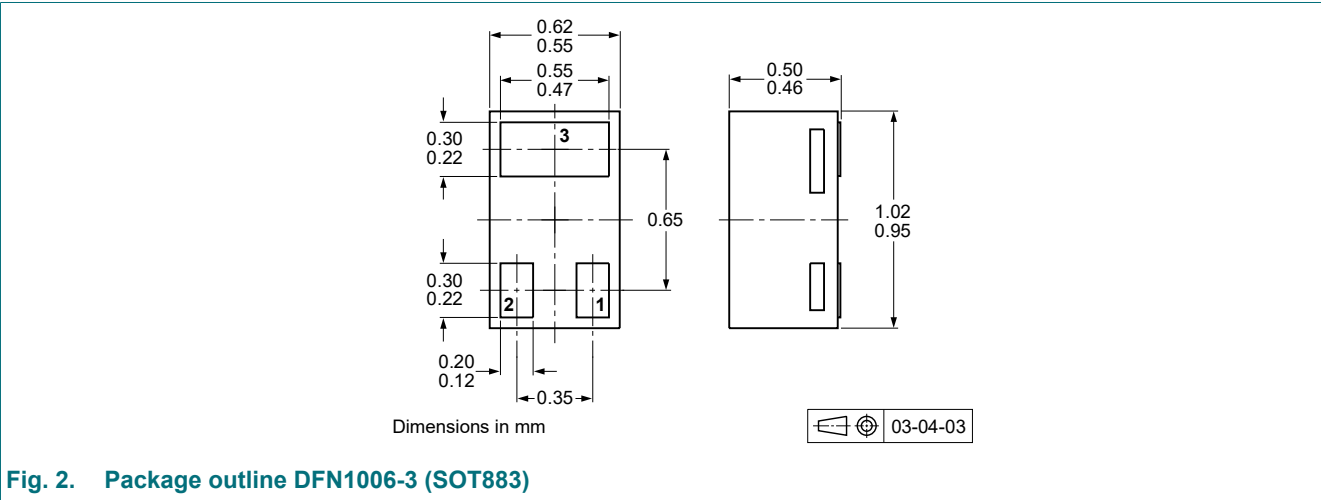
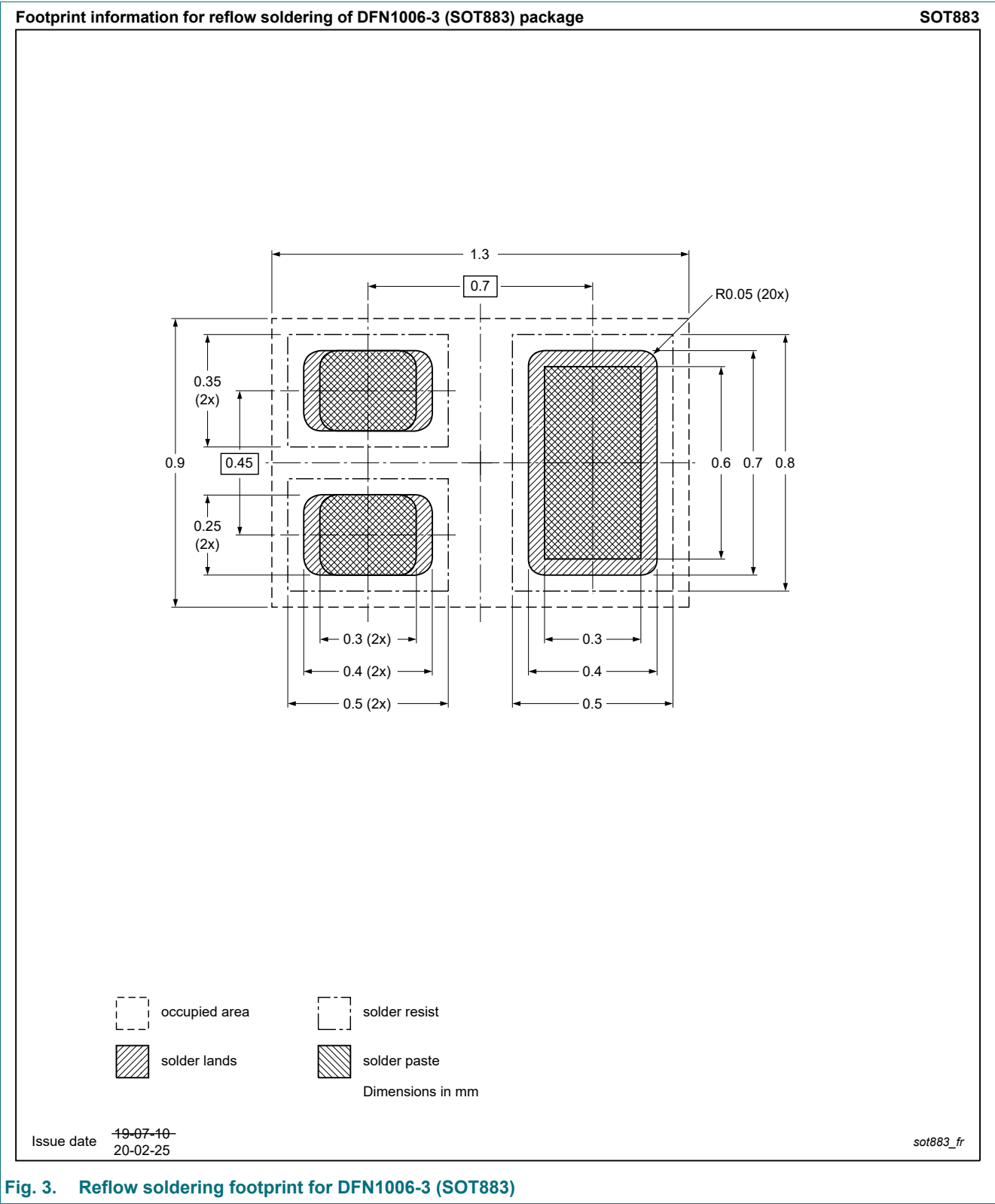


Fig. 2. Package outline DFN1006-3 (SOT883)

13. Soldering



14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTC144WM-Q v.1	20250627	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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